REMARKS

Claims 1-23 are pending in the present application. Claims 1-23 have been rejected. No new matter has been added. Accordingly, claims 1-23 are now pending in the present application.

Objection to Drawings 37 CFR 1.83(a)

The drawings are objected to under 37 CFR 1.83(a) because they fail to show pointers on how the signals are directed in figures 3 and 4 as described in the specification. Applicant has amended the drawings 3 and 4 to overcome this objection and these are designated as "Replacement Figures."

Examiner Stated:

> The drawings are objected to under 37 CFR 1.83(a) because they fail to show pointers on how the signals are directed in figures 3 and 4 as described in the specification. It is not clear how the signal is directed between the two summers 106a and 106b. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Objections to the Specification

The disclosure is objected to because of the following informalities. Please amend Specification, page 7, line 9-page 7, line 20; Line 5 as follows: "(pd1)" and Line 10, "negative input" and Specification, page 8, line 14-page 9, line 2; Line10, "atop". Applicant has amended the specification to overcome this objection.

Rejections Under 35 USC § 112

Claims 1 - 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Examiner Stated:

> Claims 1 - 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.
>
> In reviewing the specification for figure 3 in paragraphs 0025 - 0027, it is unclear for one of ordinary skill to understand the operation of the circuit shown. According to paragraph 0025, lines 1 - 2, "a negative output from summer 106a is provided to a positive input of summer 106b". It is unclear what is summed in summer 106a. As described, there is no summation involved in 106a and could be assumed that that pdOl = pd0. However, this not as recited in the claims, where the phase differences of the at least two phase detectors are summed.
>
> In reviewing the specification for figure 4, no description was found in the disclosure to enable one of ordinary skill to understand the operation of the embodiment.

ARGUMENTS

Applicant respectfully disagrees. From the Specification at page 6, lines10-page 7, line2:

"To describe the features of the present invention in more detail, refer now to the following description in conjunction with the accompany figures. Figure 3 illustrates a first embodiment of a phase-offset cancellation mechanism 100 in accordance with the present invention. Figure 4 illustrates a second embodiment of a phase cancellation circuit 200 in accordance with the present invention. As is seen, since the output of each of the phase detectors 204a-204d is a current instead of a voltage a separate phase detector per input of the summing block is required. Either of the phase-offset cancellation mechanisms 100 or 200 can be coupled to the multi-phase clock generator 10 of Figure 1 via the serial line input data line 12 to provide the appropriate phase-offset cancellation.

Each of these embodiments illustrate a four-phase system with almost equal phase spacings provides the offset cancellation scheme. The four component clock signals (cki0 to cki3) can be the output of a multi-phase generation circuit that experience phase errors due to the mismatches in the clock generation circuit and its following buffers. It should be understood that, although the present invention is described with respect to a four-phase system, the same architecture can be extended to any equally spaced multiple phase system and it would be within the spirit and scope of the present invention." Emphasis added.

The above clearly describes that Figure 4 is another embodiment of a phrase offset cancellation circuit and that the output of the detectors is a current. Otherwise the circuit 200 would be the same as circuit 100.

Applicant respectfully submits that the operation of the Phase Offset cancellation circuit is described with particularity at Specification, Page 7, line 21-Page 8, line 13 by the following:

"The phase detectors 104a-104d convert the phase difference between two component clock signals into a proportional current, and the analog subtractor within the summers 106a-106c uses the current difference from two adacent phase detectors to charge and discharge a capacitor (not shown) at is output.

Accordingly, a key feature of a preferred embodiment of the present invention is to equalize every two adjacent phase differences. Therefore, the phase of the first component clock signal, ckio, is fixed as the phase reference, and the phase of the next component clock signal, cki1, is adjusted in such a way that the phase difference between component clock signal ck0 and component clock signal ck1 (pd0) is equal to component clock signal ck1 and component clock signal ck2 (pd1). The same mechanism may be used to adjust the next clock phase ck2, and so on. Each phase detector 104a-104d measures the phase spacing of the two adjacent clocks, pdi, and the difference between pdi and pdi+1 is applied to the adjustable delay element by a subtractor to cancel the phase error of that stage. It should be noted that in alternative embodiments of the present invention, the techniques described herein may be used to equalize phase differences between any one or more pairs of component clock signals." Emphasis added.

The above clearly describes the operator of the phase-offset cancellation circuit. The summer 106a provides a negative output pd01 and an inverse of that output. Accordingly, the summer 106a receives one input and produces a positive output and a negative output. The phase detector 104a converts the phase difference between ckO and ck1. As has been described above, the phase of a first component clock signal cki0 is fixed as the phase reference and the phase of the next clock signal ckil is adjusted.

CONCLUSION

In view of the above, applicant respectfully requests reconsideration and allowance of the claims as now presented.

Applicants' attorney believes this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,

October 11, 2007

/.Joseph A. Sawyer, Jr./
Joseph A. Sawyer, Jr.
Reg. No. 30,801

Customer Number 29141
(650) 493-4540
(650) 493-4549